**Overview**

During the Spring 2023 Semester, I began my senior design project at Iowa State University. Senior Design is a two semester course, with a focus on research and design in the first semester, and then implementation in the second semester. The project that me and three other group mates are working on is called Digital ASIC Fabrication, and will involve designing and fabricating a digital ASIC. Our client and advisor will be Dr. Duwe, a professor at Iowa State who researches and teaches about computer architecture and cyber security topics. Dr. Duwe has had two previous senior design groups follow the same process and design cycle as we will, each staggered one semester apart. The first senior design team was able to successfully get their chip approved and fabricated, and we are currently waiting to receive it. If all goes well, part of our second semester goal will include bringing up the first chip developed by an earlier team.

Since we started a few weeks ago, we still do not currently have our project selected. We will be submitting our open-source project through Efabless, which is an ongoing project working towards standardizing ASIC production and open-source tooling. There are many helpful links, documents, and a slack channel full of resources for us to use, alongside the previous senior design team who is in their second semester currently. By submitting our project through Efabless, we will be able to perform the logic design, waveform testing, and hardening of a silicon chip, all in one project. I am extremely excited to see this project from start to end, and am looking forward to narrowing down our projects and beginning our planning phase.

Useful Links:

* Efabless: <https://efabless.com/>
* Open Source Tool Setup: <https://caravel-user-project.readthedocs.io/en/latest/#quickstart>
* Other projects on Efabless: <https://platform.efabless.com/projects/project_definition/1>